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| 10/727,138 | 12/03/2003 | Kaushik Saha | 852463.406 | 5322 |

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| EXAMINER | |
|---|---|
| DO, CHAT C | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/727,138 | SAHA ET AL. | |
| | Examiner | Art Unit | |
| | CHAT C. DO | 2193 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7 and 10-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/03/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This communication is responsive to Amendment filed 06/11/2008.

2. Claims 1-7 and 10-23 are pending in this application. Claims 1, 3, 5 and 16 are independent claims. In Amendment, claims 8-9 are cancelled and claims 21-23 are added. This Office Action is made non-final after a RCE filed 06/11/2008.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 21-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claim 21, the original specification does not explicitly disclose the N-point FFT/IFFT is computed without a combination phase in order to produce the result of N-point FFT/IFFT as clearly cited in the newly added limitations. Thus, the original specification does not enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention as required. Claims 22-23 have the same rejection.

***Claim Rejections - 35 USC § 101***

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-7 and 10-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-7 and 10-23 cite a method, system, product, and medium for performing a/an FFT/IFFT in accordance with a predetermined mathematical algorithm. However, claims 1-7 and 10-23 merely disclose steps/components for performing FFT/IFFT without disclosing a practical/physical application. In addition, the claims appear to preempt every substantial practical application of the idea embodied by the claims. Further, claims {3-4 and 12-15} can be seen as software module; claims 5-6 are software per se. and claims 16-20 are non-functional medium. Therefore, claims 1-7 and 10-23 are directed to non-statutory subject matter.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-7 and 10-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abel et al. (U.S. 5,991,787) in view of Jaber (U.S. 6,792,441).

Re claim 1, Abel et al. disclose in Figures 1-14 a linear scalable method for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a system (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11 discloses a FFT) using a decimation in time approach (e.g. last line of abstract and col. 13 line 65 to col. 14 line 12), comprising the steps of: computing an N-point FFT/IFFT of a signal (e.g. either seen in Figures 7-8 or Figure 11 for IFFT/FFT respectively) using a first plurality of butterfly computational stages (e.g. Figure 4 and Figure 8 wherein the first plurality of butterfly is performed in components 800 and 805), each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix (e.g. Figure 8 wherein components 800 and 805 each utilizes radix-2 as the first radix size) wherein each of the butterfly operations in each stage (e.g. components 800, 805, and 810 in Figure 8) in the first plurality of stages has a single, un-nested computation loop of the first radix (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT); and storing the transformed signal (e.g. Figures 15-16 and col. 13 lines 10-45).

Abel et al. fail to disclose in Figures 1-14 the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage. However, Jaber discloses in Figures 8-9 the multiprocessing system (e.g. Figure 8 or Figure 9 as multiprocessing system for FFT/IFFT) for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes

an equal number of complete butterfly operations thereby eliminating data interdependency in the stage (e.g. abstract and col. 3 lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and simultaneously (e.g. abstract and summary of the invention in cols. 3-4).

Re claim 2, Abel et al. fail to disclose in Figures 1-14 step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor. However, Jaber discloses in Figures 8-9 step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor (e.g. col. 7 lines 2-30).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required

for each specific butterfly operation assigned to the processor as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 3, it is a system claim having similar limitations of claim 1. Thus, claim 3 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 4, it is a system claim having similar limitations of claim 2. Thus, claim 4 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 5, it is a program product claim having similar limitations of claim 8. Thus, claim 5 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 6, it has similar limitations cited in claim 2. Thus, claim 6 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 9, Abel et al. further disclose in Figures 1-14 the first plurality of stages comprises $\log_2 N$-2 stages (e.g. Figure 4 and Figure 8).

Re claim 10, Abel et al. further disclose in Figures 1-14 an output of a last stage in the first plurality of stages provides the computed N-point FFT/IFFT (e.g. output of Figure 4 or Figure 8).

Re claim 11, Abel et al. fail to disclose in Figures 1-14 the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location. However, Jaber discloses in Figures 8-9 the assigning addresses to each processor

comprises inserting a binary digit in an address of a memory location (e.g. col. 15 lines 4-35).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 12, it is a system claim having similar limitations of claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, it is a system claim having similar limitations of claim 8. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 14, it is a system claim having similar limitations of claim 9. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 15, it is a system claim having similar limitations of claim 11. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 16, it is a computer-readable memory claim having similar limitations of claim 1. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, it is a computer-readable memory claim having similar limitations of claim 2. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 18, it is a computer-readable memory claim having similar limitations of claim 11. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 19, it is a computer-readable memory claim having similar limitations of claim 9. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 20, it is a computer-readable memory claim having similar limitations of claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 21, Abel et al. further disclose in Figures 1-14 the N-point FFT/IFFT is computed without a combination phase (e.g. any Figures 1-14).

Re claim 22, it is a system claim having similar limitations of claim 21. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 21.

Re claim 23, it is a computer-readable memory medium claim having similar limitations of claim 21. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 21.

***Response to Amendment***

9. The amendment filed 06/11/2008 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Re claims 21-23, these claims cite the limitation of "computation of FFT/IFFT is performed without a combination phase". This limitation is not clearly found or supported in the original specification.

Applicant is required to cancel the new matter or clearly address how this limitation is clearly or directly seen in the original specification in the reply to this Office Action.

***Response to Arguments***

10. Applicant's arguments filed 06/11/2008 have been fully considered but they are not persuasive.

a. The applicant argues in pages 7-8 for claims rejected under 35 U.S.C. 101 that claim 1 and its dependent are directed to a multiprocessing system, claim 3 and its dependent are directed to a means-plus-function language which recites a multiprocessing

system with direct access to memory; and claims 5 and 16 and its dependent are directed to computer-readable medium. Thus, these claims are directed to statutory subject matter.

The examiner respectfully submits that all the claims are just merely directed to a mathematical FFT operations in parallel processing. It does not disclose a practical application and the method claims do not disclose a specific hardware structure for carrying the mathematical FFT operations. The original specification does not clearly or directly disclose definition of the means-plus-function language which directed to hardware structure as alleged by the applicant. Similarly, the original specification, the claim language, and even the argument do not provide any specific tangible medium for storing.

b. The applicant argues in page 9 second and third paragraphs for claims rejected under 35 U.S.C. 103(a) that the cited reference by Abel et al. does not qualify as primary reference since Abel et al. is directed to a way of reducing peak spectral error for a specific processor instead of a linear scalability as required by the cited claimed invention.

The examiner respectfully submits that the primary reference by Abel does disclose the linear scalable method of performing FFT/IFFT as clearly seen in Figure 7 wherein input data coefficients can be any size. In addition or alternative to the response, the recitation "a linear scalable method" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any

patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). The applicant is required to specific clearly the definition of the linear scalability directly in the body of the claim in order for the examiner to address in the cited reference.

c. The applicant argues in page 10 second paragraph for newly added claims that the current invention does not use the combination phase to form the final result.

The examiner respectfully submits that this limitation above is newly added and considered as new subject matter. In addition, the primary reference by Abel et al. does not need the combination phase in order to form the result of FFT operations, particularly the first stage of butterfly operations.

d. The applicant argues in pages 10-11 for claims that neither Abel nor Jaber teach, suggest, or motivate a linear scalable system as cited in the claimed invention.

The examiner respectfully submits that it is unclear as what the applicant attempts to argue since the rejection clearly states the teaching, suggestion, or motivation to combine the references to meet the claimed invention. The primary reference by Abel et al. alone clearly disclose most limitations cited in claims including a linear scalable method for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform

(IFFT) in a system (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11 discloses a FFT) using a decimation in time approach (e.g. last line of abstract and col. 13 line 65 to col. 14 line 12), comprising the steps of: computing an N-point FFT/IFFT of a signal (e.g. either seen in Figures 7-8 or Figure 11 for IFFT/FFT respectively) using a first plurality of butterfly computational stages (e.g. Figure 4 and Figure 8 wherein the first plurality of butterfly is performed in components 800 and 805), each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix (e.g. Figure 8 wherein components 800 and 805 each utilizes radix-2 as the first radix size) wherein each of the butterfly operations in each stage (e.g. components 800, 805, and 810 in Figure 8) in the first plurality of stages has a single, un-nested computation loop of the first radix (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT); and storing the transformed signal (e.g. Figures 15-16 and col. 13 lines 10-45). The only missing features/limitations in the primary reference by Abel et al. are the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage. However, these features/limitations are clearly taught, suggested, or motivated in Jaber's reference wherein Jaber discloses in Figures 8-9 the multiprocessing system (e.g. Figure 8 or Figure 9 as multiprocessing system for FFT/IFFT) for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage (e.g. abstract

and col. 3 lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

August 18, 2008